

FIG. 1

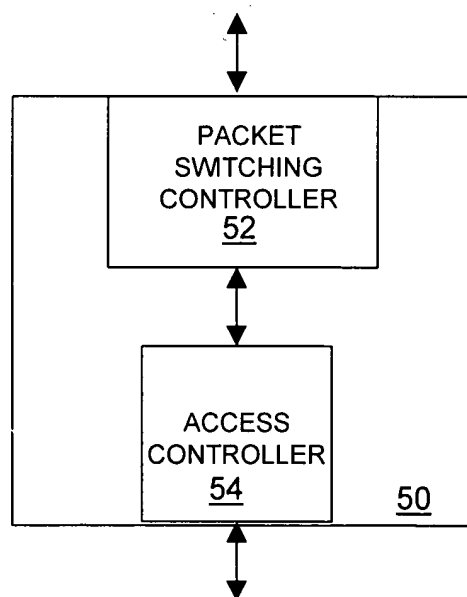


FIG. 2

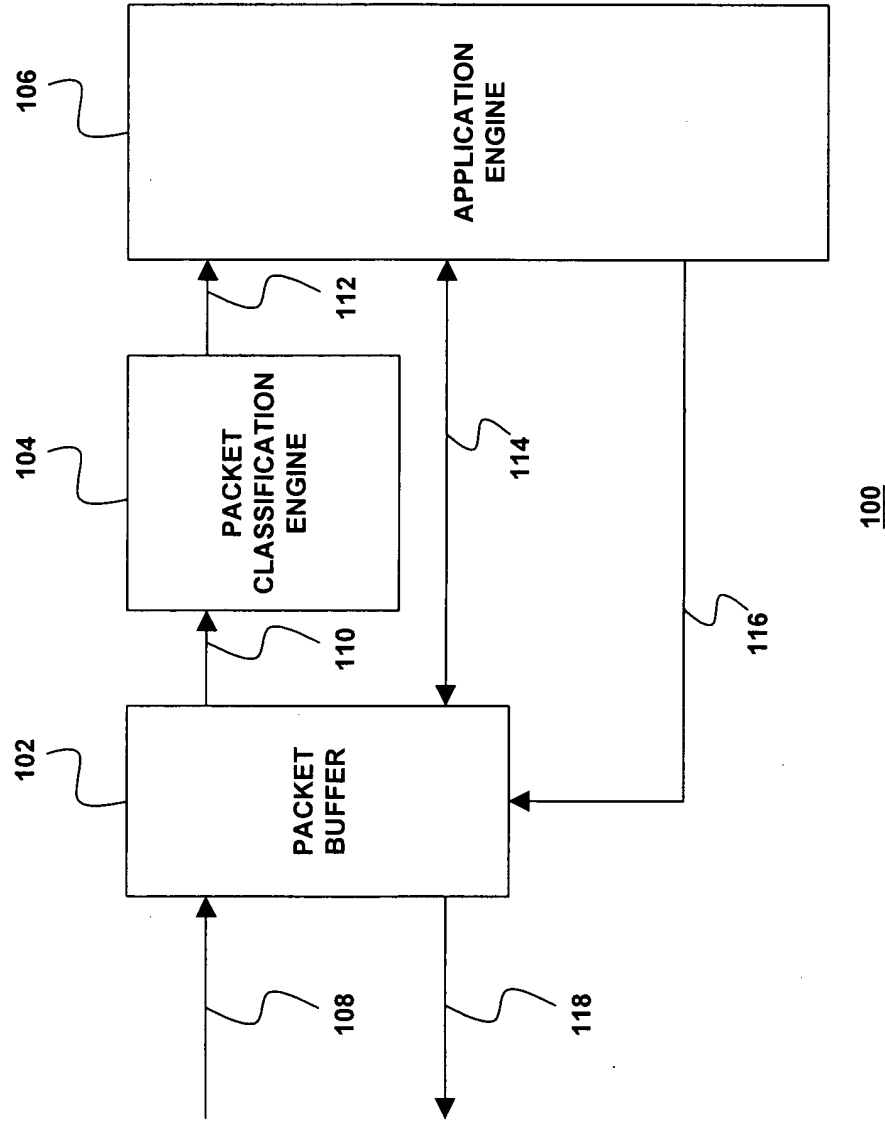
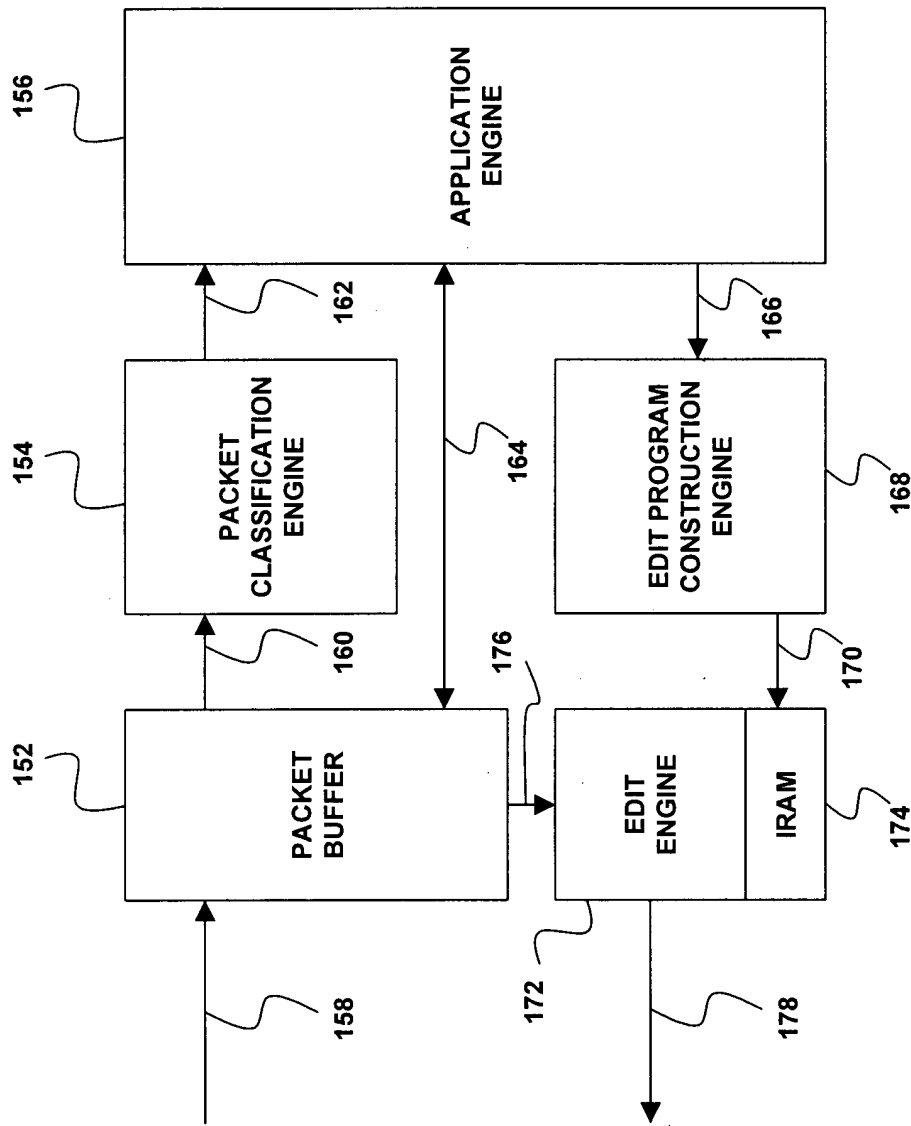


FIG. 3

FIG. 4 is a block diagram of a system 150 for processing packets. The system 150 includes a packet buffer 152, a packet classification engine 154, an application engine 156, an edit engine 172, an IRAM 174, and an edit program construction engine 168. The packet buffer 152 receives packets 158 and outputs packets 160 to the packet classification engine 154. The packet classification engine 154 outputs packets 162 to the application engine 156. The application engine 156 outputs packets 166 to the edit program construction engine 168. The edit program construction engine 168 outputs packets 170 to the IRAM 174. The IRAM 174 outputs packets 172 to the edit engine 172. The edit engine 172 outputs packets 178 to the packet buffer 152. The packet buffer 152 also outputs packets 176 to the application engine 156. The application engine 156 also outputs packets 164 to the edit engine 172.



150

FIG. 4

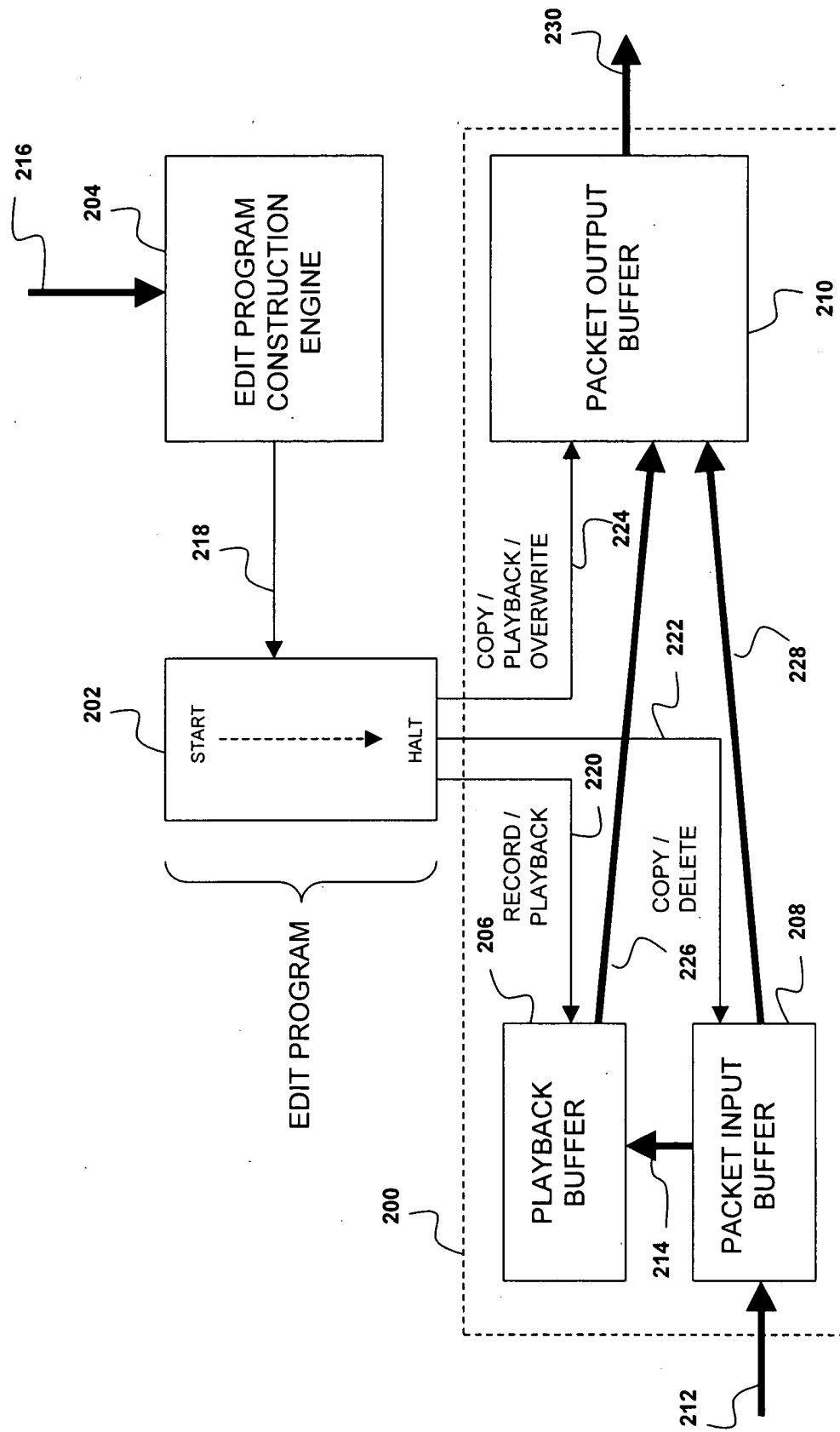


FIG. 5

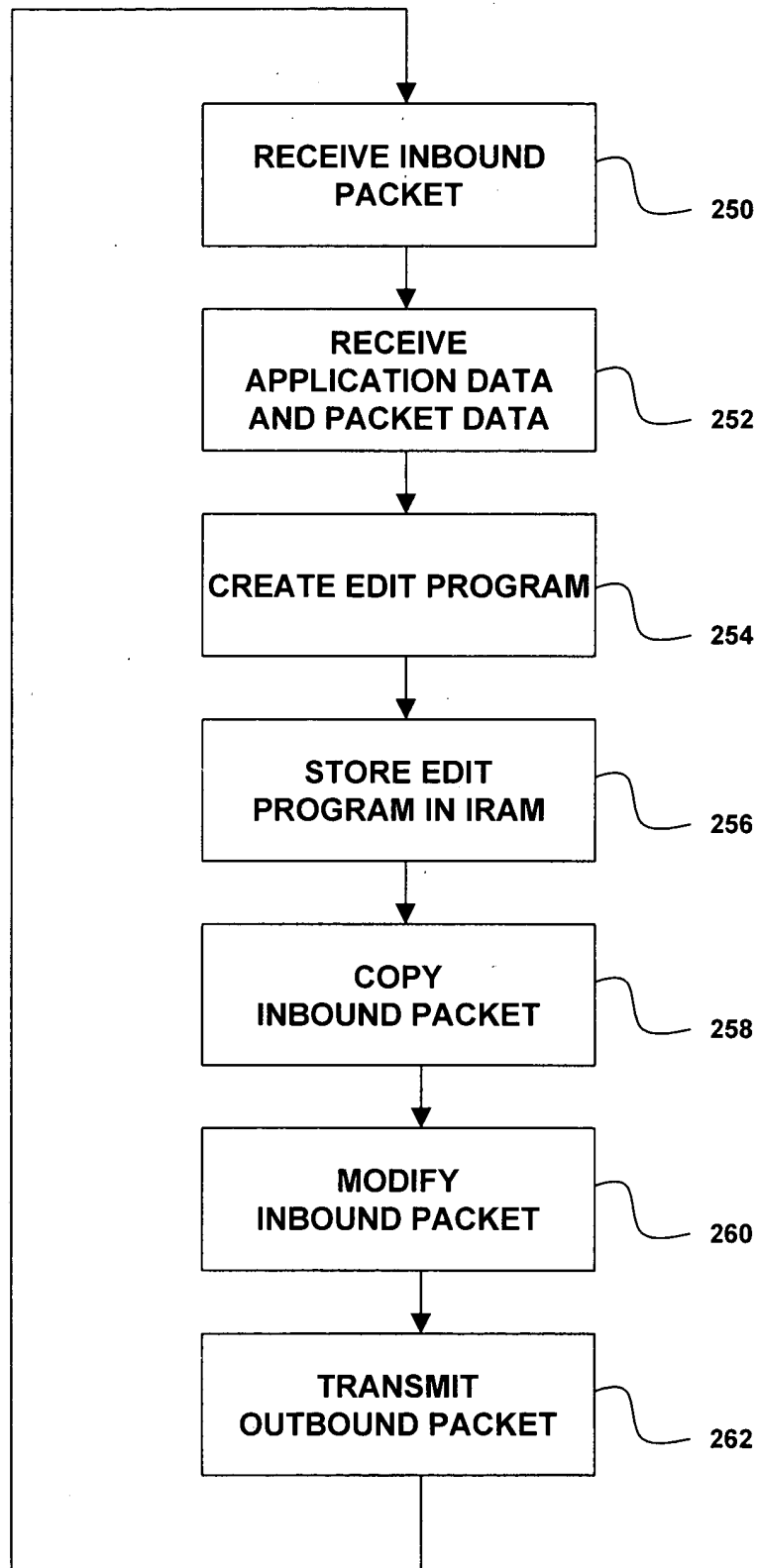


FIG. 6